

TRANSISTOR STRUCTURE HAVING REDUCED TRANSISTOR LEAKAGE
ATTRIBUTES

Abstract of the Disclosure

5 Undesirable transistor leakage in transistor structures becomes greatly reduced
in substrates having a doped implant region formed via pulling back first and second
layers of a process stack. A portion of the substrate, which also has first and second
layers deposited thereon, defines the process stack. The dopant is selected having the
same n- or p- typing as the substrate. Through etching, the first and second layers of
10 the process stack become pulled back from a trench wall of the substrate to form the
implant region. Occupation of the implant region by the dopant prevents undesirable
transistor leakage because the electrical characteristics of the implant region are so
significantly changed, in comparison to central areas of the substrate underneath the
first layer, that the threshold voltage of the implant region is raised to be about
15 equivalent to or greater than the substantially uniform threshold voltage in the central
area.

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